

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Xisheng Zhang et al.  
Assignee: Cadence Design Systems, Inc.  
Title: MOSFET Modeling for IC Design Accurate for High Frequencies  
Application No.: Unknown Filing Date: Herewith  
Examiner: Unknown Group Art Unit: Unknown  
Docket No.: BTAT.001US1 Conf. No.: Unknown

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MAIL STOP PATENT APPLICATION  
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**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are not enclosed, since they were either previously submitted in the parent Application No. 09/661,328, or cited by the Examiner in that application.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made a representation that a search has been made, (other than as indicated by any cited document); or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

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Respectfully submitted,



Michael G. Cleveland  
Patent Agent  
Reg. No. 46,030

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.	Serial No.			
				M-10095 US	09/661,328			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT  (Use several sheets if necessary)				Applicant(s)				
				Zhang et al.				
				Filing Date	Group			
				September 14, 2001	2812			
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	X. Jin, "An Effective Gate resistance Model for CMOS RF and Noise Modeling", Digest of Technical Papers IEDM-98, December 1998, pages 961-9694.						
	AR	S.F. Tin et al., "A Simple Subcircuit Extension of the BSIM3V3 Model of CMOS RF Design," IEEE Journal of Solid -State Circuits, Vol. 35, No. 4, April 2000, pp. 612 623.						
	AS	W. Liu et al., "RF MOSFET Modeling Accounting for Distributed Substrate and Channel Resistance with Emphasis on BSIM3V3 SPICE Model", Digest of Technical Papers IEDM-97, December 1997, pages 309-312.						
Examiner		Date Considered						
<p><b>*EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								

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	AQ	S.H. Jen et al., "Accurate Modeling and Parameter Extraction of MOS Transistors up to 10 GHz," IEEE Transactions on Electronic Devices, Vol. 46, No. 11, November 1999, pp. 2217-2227.						
	AR	C. Enz et al., "MOS Transistor Modeling for RF IC Design," IEEE Transactions on Solid-State Circuit, Vol. 35, No. 2, February 2000, pp. 186-2001						
	AS	M.E. Mokari et al., "A New Method of Noise Parameter Calculation Using Direct Matrix Analysis," IEEE Transactions on Circuits and Systems-1: Fundamental Theory and Applications, Vol. 39, No. 9, September 1992, pp. 767-771.						
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	AQ	T.E. Kolding, "Test Structure for Universal Estimation of MOSFET Substrate Effects at Gigahertz Frequencies," IEEE International Conference on Microelectronic Test Structures, March 2000, pp. 106-111.						
	AR	C.C. Su et al., "A Monolithic 2.4 GHz CMOS Active Balanced Circuit," IEEE, Vol. 2, November 1999, pp. 214-217.						
	AS	K. H. Kim et al., "Full Software Analysis and Impedance Matching of Radio Frequency CMOS Integrated Circuits," IEEE Transactions on Components and Packaging Technologies, Vol. 23, No. 1, March 2000, pp. 183-189.						
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	AQ	Hi-Deok Lee et al., "Characterization of Crosstalk-Induced Noise for 0.18 $\mu$ M CMOS Technology with 6-Level Metalization Using Time Domain Reflectometry and S. Parameters," IEEE: International Electronic Devices Meeting, December 5, 1999, pp. 37.4.1-37.4.4.					
	AR	J. J. Ou et al., "Submicron CMOS Thermal Noise Modeling from an RF Perspective," IEEE Symposium on VLSI Technology Digest of Technical Papers, 1999, pp151-152.					
	AS	J. Zheng et al., "CAD-Oriented Equivalent Circuit Modeling of On-Chip Interconnects for RF Integrated Circuits in CMOS Technology," IEE MTT-S International Microwave Symposium Digest, June, 1999, Vol. 1, pp. 35-38.					
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	AQ	Behzad Razavi, "CMOS Technology Characterization for Analog and RF Design," IEEE Journal of Solid-State Circuits, Vol. 34, No. 3, pp.268-276.						
	AR	Behzad Razavi, "CMOS Technology Characterization for Analog and RF Design," IEEE Custom Integrated Circuits Conference, 1998, pp. 3.1.1-3.1.8.						
	AS	W.S. Kwan et al., "Hot-Carrier Effects on the Scattering of Lightly Doped Drain N-Type Metal-Oxide-Semiconductor Field Effects Transistors," Journal of Vacuum Science and Technology B: Micro Electronics and Nanometer Structures, Vol. 16, No. 2, pp. 628-632.						
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	AQ	C. E. Biber et al., "Improvements on a MOSFET Model for Non-Linear RF Simulations," 1997 IEEE MTT-S International Microwave Symposium Digest, June, 1997, Vol. 2, pp. 865-868.						
	AR	Jin-Young Choi et al., "Effects of Substrate Resistance on Microwave Characteristics of MOS Transistors," Journal of Electrical Engineering and Information Science, 1999, Volume 4, No. 2, pp. 244-248.						
	AS	Jin-Young Choi, "Macro Modeling of MOS Transistors for RF Applications," Journal of the Institute of Electronics Engineers of Korea, 1999, Vol. 36-D, No. 5, pp. 54-62.						
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	AQ	Weidong Liu et al., "PSIM4.0.0 MOSFET Model-User's Manual," UC Berkeley-Department of Electrical Engineering and Computer Sciences, 2000, pp. 1.1-13.14.						
	AR	Hewlett-Packard Application Note 57-1, "Fundamentals of RF and Microwave Noise Figure Measurements," pp. 1-40.						
	AS	Lawrence T. Pillage et al., "Simulation of Nonlinear Circuits," <u>Electronic Circuit and System Simulation Methods</u> , 1994, Chapter 10, pp. 285-314.						
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